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**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions and listings of claims in the application:

**LISTING OF CLAIMS**

1. - 5. (canceled)
6. (original) A method of confusing a reverse engineer comprising the steps of:
  - providing a false semiconductor device without sidewall spacers having at least one active region; and
  - forming a conductive layer partially over the at least one active region such that an artifact edge of said conductive layer of said false semiconductor device without sidewall spacers mimics an artifact edge of a conductive layer of a semiconductor device having sidewall spacers.
7. (original) The method of claim 6 wherein the conductive layer is a silicide layer.
8. (original) The method of claim 6 wherein the false semiconductor device is a false transistor having a polysilicon gate and wherein the step of forming a conductive layer comprises the step of modifying a conductive layer block mask such that the artifact edge of said conductive layer is offset from an edge of said polysilicon gate.
9. (original) The method of claim 8 wherein the offset between the artifact edge of said conductive layer and said edge of said polysilicon gate is approximately equal to a width of a sidewall spacer.
10. (original) A method of camouflaging a non-operational circuit structure comprising the steps of:
  - forming the non-operational circuit structure having a plurality of active areas;
  - and

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forming a conductive block layer mask to thereby form an artifact edge of a conductive layer that is located in a same relative location for the non-operational circuit structure without sidewall spacers as an operational circuit structure with sidewall spacers.

11. (original) The method according to claim 10 wherein the conductive layer is a silicide layer.

12. (original) A method of protecting an integrated circuit design comprising:

modifying a silicide block mask used during the manufacture of a false transistor such that edges of a silicide layer for the false transistor are placed in substantially the same relative locations as edges of a silicide layer for a true transistor; and  
manufacturing said integrated circuit.

13. - 15. (canceled)

16. (original) A method of hiding a circuit function of a circuit, the method comprising the steps of:

forming at least one active region of a device with a single processing step, said at least one active region having a width; and

forming a conductive layer partially over the at least one active region wherein a width of said conductive layer is less than the width of the at least one active region so that the conductive layer yields an artifact edge, when subjected to reverse engineering techniques, which is in a conventionally anticipated location for a conventionally operational version of the circuit, but wherein the circuit, due to the width of the at least one active region, functions in an unanticipated fashion.

17. (original) The method of claim 16 wherein said device is non-operable.

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18. (original) The method of claim 16 wherein a difference between the width of the at least one active region and the width of the conductive layer is approximately equal to a width of a sidewall spacer.

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